Amendments to the Claims

Claim 1 **(Currently Amended)** A signal processor for subjecting data read from a recording medium to predetermined digital signal processing, and subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block, said signal processor comprising:

a first memory operable to sequentially store the data which has been subjected to the predetermined digital signal processing;

an error correction block operable to subject the data, which has been stored in said first memory, to error correction for each predetermined error correction block;

a second memory;

a descrambling/error detection block operable to read the data after the error correction from said first memory, descramble the data which has been subjected to the error correction, detect errors in the data after the descrambling, and thereafter store the data in said second memory; and

a controller operable to transmit error-free data which has been stored in said second memory to a host computer when said descrambling/error detection block judges that there is no error in the data which has been stored in said second memory,

wherein, when said descrambling/error detection block judges that there is an error in the data stored in said second memory, the data stored in said second memory are read out for each predetermined error correction block, and subjected to error correction by said error correction block.

Claim 2 **(Previously Presented)** A signal processor as described in Claim 1, wherein said error correction block comprises:

a syndrome calculator operable to calculate syndrome of the data which has been subjected to the predetermined digital signal processing;

an error position/pattern calculator operable to calculate an error position and an error pattern after the syndrome calculation;

an error correction result holding block operable to hold information as to whether or not the data detected by said error position/pattern calculator is error-correctable;

a data correction block operable to read erroneous data stored in said first memory, correct errors in the data, and store the data which has been subjected to the error correction in said first memory based on the error position and the error pattern calculated by said error position/pattern calculator; and

a number-of-error-correction control block operable to control a number of error corrections.

Claim 3 **(Previously Presented)** A signal processor as described in Claim 1, wherein said descrambling/error detection block comprises:

a first memory interface operable to read the data stored in said first memory;

a descrambling block operable to descramble the data after the error correction which has been read from said first memory;

an error detection block operable to detect errors in the descramble data;

a second memory interface operable to store the descramble data in said second memory; and

an error detection result holding block operable to hold a result of the error detection as to whether there is any error in the data which has been subjected to the error detection.

Claim 4 **(Canceled)**